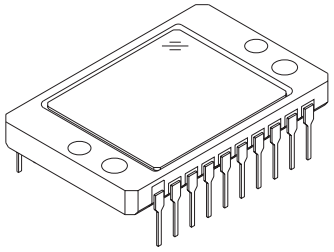
SONY

ICX285AQ

Diagonal 11mm (Type 2/3) Progressive Scan CCD Image Sensor with Square Pixel for Color Cameras

20 pin DIP (Ceramic)



Description

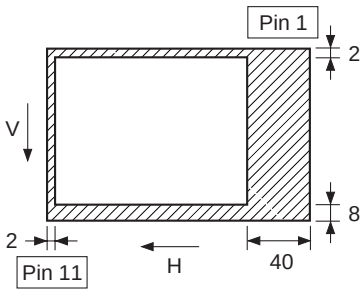
The ICX285AQ is a diagonal 11mm (Type 2/3) interline CCD solid-state image sensor with a square pixel array. High sensitivity and low smear are achieved through the adoption of EXview HAD CCD technology. Progressive scan allows all pixels' signals to be output independently within approximately 1/15 second. Also, the adoption of high frame rate readout mode supports 60 frames per second. This chip features an electronic shutter with variable charge-storage time which makes it possible to realize full-frame still images without a mechanical shutter.

High resolution and high color reproductively are achieved through the use of R, G, B primary color mosaic filters.

This chip is suitable for image input applications such as still cameras which requires high resolution, etc.

Features

- Progressive scan allows individual readout of the image signals from all pixels.
- High horizontal and vertical resolution (both approximately 800 TV-lines) still images without a mechanical shutter
- Supports high frame rate readout mode (effective 256 lines output, 60 frames/s)
- Square pixel
- Aspect ratio : 4:3
- Horizontal drive frequency: 28.64MHz
- R, G, B primary color mosaic filters on chip
- High sensitivity, low smear
- Low dark current, excellent anti-blooming characteristics
- Continuous variable-speed shutter function
- Horizontal register: 5.0V drive



Optical black position (Top View)

Device Structure

- Interline CCD image sensor
- Image size: Diagonal 11mm (Type 2/3)
- Total number of pixels: 1434 (H) × 1050 (V) approx. 1.50M pixels
- Number of effective pixels: 1392 (H) × 1040 (V) approx. 1.45M pixels
- Number of active pixels: 1360 (H) × 1024 (V) approx. 1.40M pixels
- Chip size: 10.2mm (H) × 8.3mm (V)
- Unit cell size: 6.45µm (H) × 6.45µm (V)
- Optical black: Horizontal (H) direction: Front 2 pixels, rear 40 pixels
  Vertical (V) direction: Front 8 pixels, rear 2 pixels
- Number of dummy bits: Horizontal 20
  Vertical 3
- Substrate material: Silicon

***EXview* HAD CCD** TM

* EXview HAD CCD is a trademark of Sony Corporation.
EXview HAD CCD is a CCD that drastically improves light efficiency by including near infrared light region as a basic structure of HAD (Hole-Accumulation-Diode) sensor.

E01420B3Z

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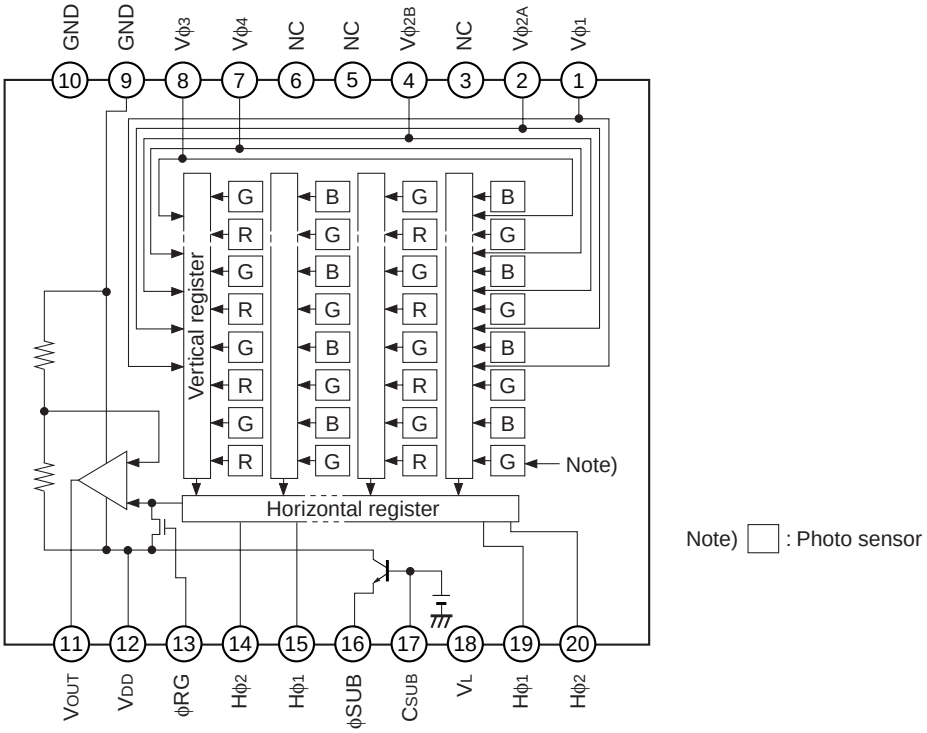
Block Diagram and Pin Configuration (Top View)



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vφ1	Vertical register transfer clock	11	V_{OUT}	Signal output
2	Vφ2A	Vertical register transfer clock	12	V_{DD}	Supply voltage
3	NC		13	φRG	Reset gate clock
4	Vφ2B	Vertical register transfer clock	14	Hφ2	Horizontal register transfer clock
5	NC		15	Hφ1	Horizontal register transfer clock
6	NC		16	φSUB	Substrate clock
7	Vφ4	Vertical register transfer clock	17	C_{SUB}	Substrate bias*1
8	Vφ3	Vertical register transfer clock	18	V_L	Protective transistor bias
9	GND	GND	19	Hφ1	Horizontal register transfer clock
10	GND	GND	20	Hφ2	Horizontal register transfer clock

*1 DC bias is generated within the CCD, so that this pin should be grounded externally through a capacitance of 0.1µF.

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Against φSUB	V_{DD}, V_{OUT}, φRG – φSUB	–40 to +12	V	
	$V\phi_{2A}$, $V\phi_{2B}$ – φSUB	–50 to +15	V	
	$V\phi_1$, $V\phi_3$, $V\phi_4$, V_L – φSUB	–50 to +0.3	V	
	$H\phi_1$, $H\phi_2$, GND – φSUB	–40 to +0.3	V	
	C_{SUB} – φSUB	–25 to	V	
Against φGND	V_{DD}, V_{OUT}, φRG, C_{SUB} – GND	–0.3 to +22	V	
	$V\phi_1$, $V\phi_{2A}$, $V\phi_{2B}$, $V\phi_3$, $V\phi_4$ – GND	–10 to +18	V	
	$H\phi_1$, $H\phi_2$ – GND	–10 to +6.5	V	
Against ϕV_L	$V\phi_{2A}$, $V\phi_{2B}$ – V_L	–0.3 to +28	V	
	$V\phi_1$, $V\phi_3$, $V\phi_4$, $H\phi_1$, $H\phi_2$, GND – V_L	–0.3 to +15	V	
Between input clock pins	Voltage difference between vertical clock input pins	to +15	V	*1
	$H\phi_1$ – $H\phi_2$	–6.5 to +6.5	V	
	$H\phi_1$, $H\phi_2$ – $V\phi_4$	–10 to +16	V	
Storage temperature		–30 to +80	°C	
Guaranteed temperature of performance		–10 to +60	°C	
Operating temperature		–10 to +75	°C	

*1 +24V (Max.) when clock width < 10µs, clock duty factor < 0.1%.
+16V (Max.) is guaranteed for turning on or off power supply.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}	14.55	15.0	15.45	V	
Protective transistor bias	V_L	*2				
Substrate clock	φSUB	*3				
Reset gate clock	φRG	*3				

*2 V_L setting is the V_{VL} voltage of the vertical clock waveform, or the same voltage as the V_L power supply for the V driver should be used.

*3 Do not apply a DC bias to the substrate clock and reset gate clock pins, because a DC bias is generated within the CCD.

DC Characteristics

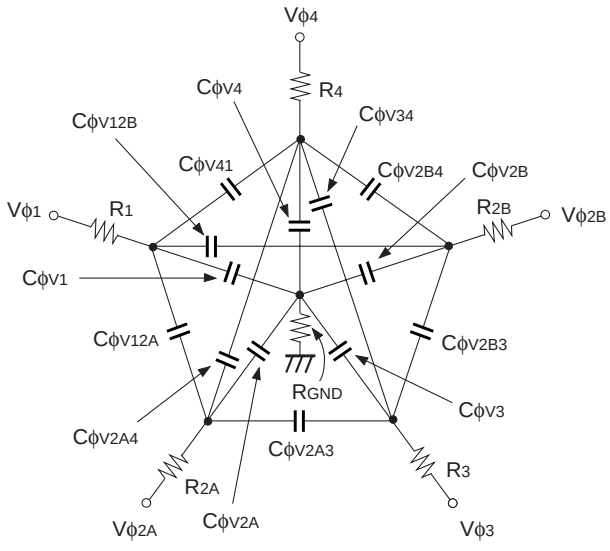
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current	I_{DD}		9	11	mA	

Clock Voltage Conditions

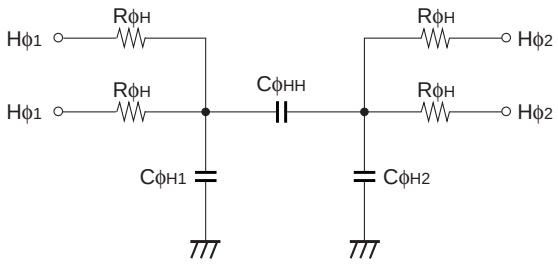
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform Diagram	Remarks
Readout clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2}	–0.05	0	0.05	V	2	$V_{VH} = (V_{VH1} + V_{VH}) /2$
	V_{VH3}, V_{VH4}	–0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	–7.3	–7.0	–6.7	V	2	$V_{VL} = (V_{VL3} + V_{VL}) /2$
	$V\phi_V$	6.5	7.0	7.35	V	2	$V\phi_V = V_{VH}n – V_{VL}n$ (n = 1 to 4)
	$V_{VH3} – V_{VH}$	–0.25		0.1	V	2	
	$V_{VH4} – V_{VH}$	–0.25		0.1	V	2	
	V_{VHH}			1.4	V	2	High-level coupling
	V_{VHL}			1.3	V	2	High-level coupling
	V_{VLH}			1.4	V	2	Low-level coupling
	V_{VLL}			0.8	V	2	Low-level coupling
Horizontal transfer clock voltage	$V\phi_H$	4.75	5.0	5.25	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
	V_{CR}	$V\phi_H/2$			V	3	Cross-point voltage
Reset gate clock voltage	$V\phi_{RG}$	3.0	3.3	5.5	V	4	
	$V_{RGLH} – V_{RGLL}$			0.4	V	4	Low-level coupling
	$V_{RGL} – V_{RGLm}$			0.5	V	4	Low-level coupling
Substrate clock voltage	$V\phi_{SUB}$	21.25	22.0	22.75	V	5	

Clock Equivalent Circuit Constants

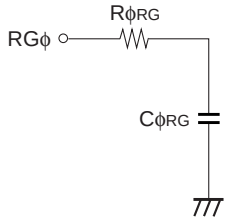
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$		5600		pF	
	$C_{\phi V2A}$		6800		pF	
	$C_{\phi V2B}$		22000		pF	
	$C_{\phi V3}$		8200		pF	
	$C_{\phi V4}$		22000		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12A}$		150		pF	
	$C_{\phi V12B}$		390		pF	
	$C_{\phi V2A3}$		270		pF	
	$C_{\phi V2B3}$		470		pF	
	$C_{\phi V14}$		2200		pF	
	$C_{\phi V34}$		330		pF	
	$C_{\phi V2A4}$		390		pF	
	$C_{\phi V2B4}$		560		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$		47		pF	
	$C_{\phi H2}$		39		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		74		pF	
Capacitance between reset gate clock and GND	$C_{\phi RG}$		4		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		1300		pF	
Vertical transfer clock series resistor	R_1, R_3		30		Ω	
	R_{2A}, R_{2B}		32		Ω	
	R_4		20		Ω	
Vertical transfer clock ground resistor	R_{GND}		60		Ω	
Horizontal transfer clock series resistor	$R_{\phi H}$		7.5		Ω	
Reset gate clock ground resistor	$R_{\phi RG}$		24		Ω	



Vertical transfer clock equivalent circuit



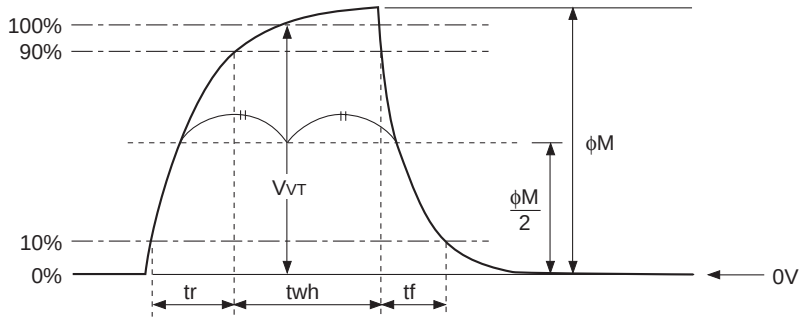
Horizontal transfer clock equivalent circuit



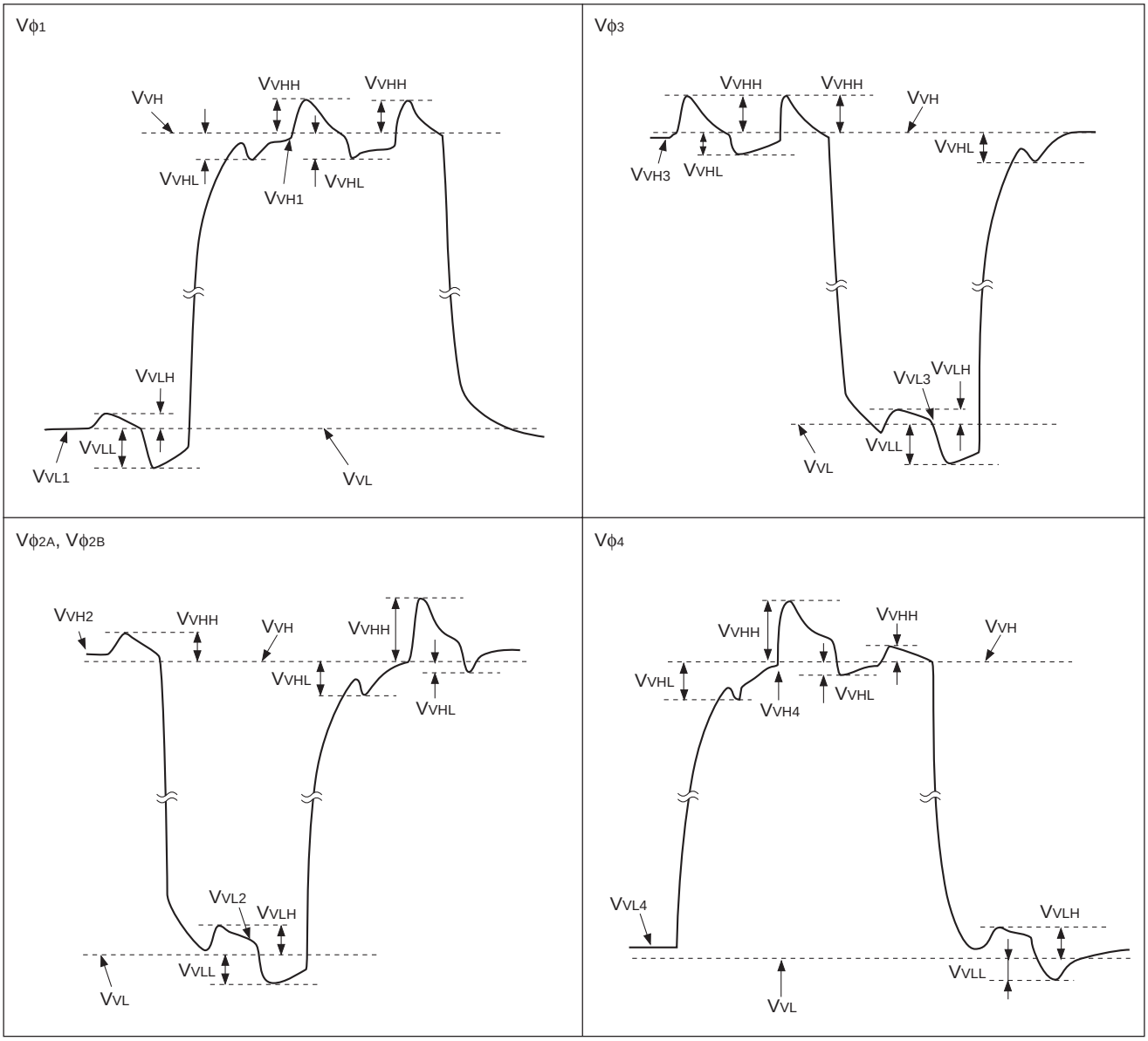
Reset gate clock equivalent circuit

Drive Clock Waveform Conditions

(1) Readout clock waveform



(2) Vertical transfer clock waveform

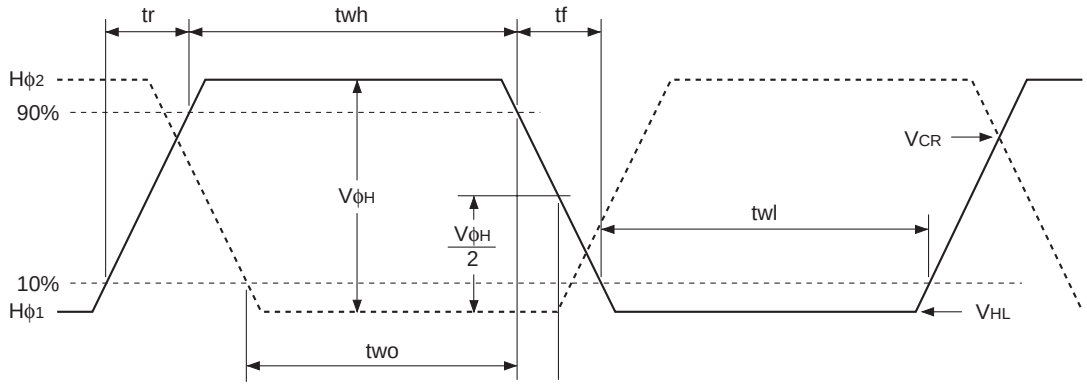


$V_{VH} = (V_{VH1} + V_{VH2}) /2$

$V_{VL} = (V_{VL3} + V_{VL4}) /2$

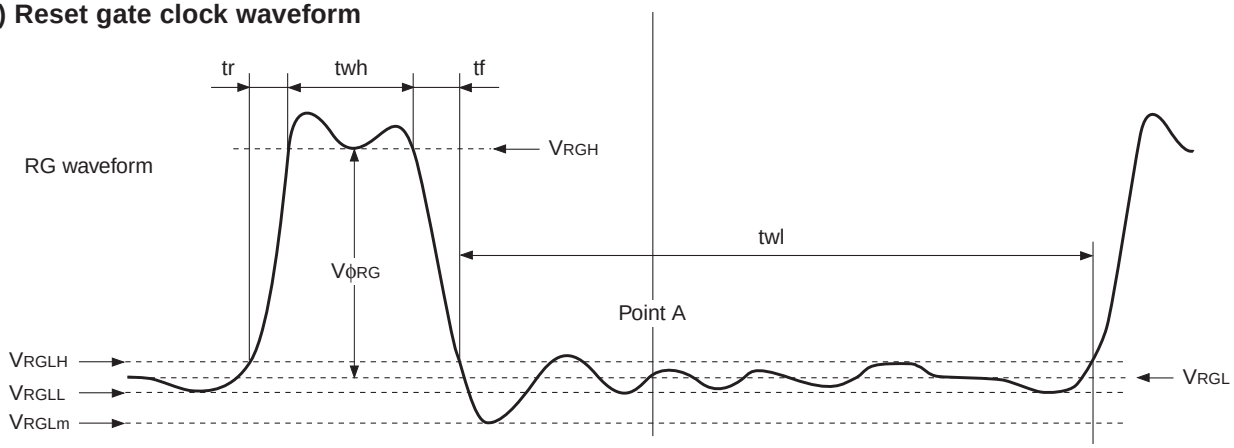
$V_{\phi V} = V_{VHn} – V_{VLn}$ (n = 1 to 4)

(3) Horizontal transfer clock waveform



Cross-point voltage for the Hφ1 rising side of the horizontal transfer clocks Hφ1 and Hφ2 waveforms is VCR.
The overlap period for twh and twl of horizontal transfer clocks Hφ1 and Hφ2 is two.

(4) Reset gate clock waveform



VRGLH is the maximum value and VRGLL is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG.
In addition, VRGL is the average value of VRGLH and VRGLL.

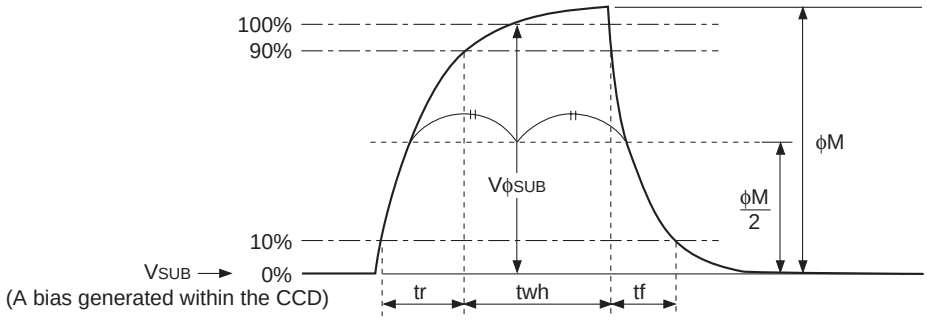
$$V_{RGL} = (V_{RGLH} + V_{RGLL}) / 2$$

Assuming VRGH is the minimum value during the interval with twh, then:

$$V_{\phi RG} = V_{RGH} - V_{RGL}$$

Negative overshoot level during the falling edge of RG is VRGLm.

(5) Substrate clock waveform



Clock Switching Characteristics (Horizontal drive frequency: 28.64MHz)

Item		Symbol	twh			twl			tr			tf			Unit	Remarks
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock		V_T	2.8	3.0						0.5			0.5		µs	During readout
Vertical transfer clock		$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$										15		250	ns	When using CXD3400N
Horizontal transfer clock	During imaging	$H\phi_1$	10	12.5		10	12.5			5	7.5		5	7.5	ns	tf ≥ tr – 2ns
		$H\phi_2$	10	12.5		10	12.5			5	7.5		5	7.5		
	During parallel-serial conversion	$H\phi_1$								0.01			0.01		µs	
		$H\phi_2$								0.01			0.01			
Reset gate clock		ϕRG	4	8			24			2			2		ns	
Substrate clock		ϕSUB	3.5	3.9							0.5			0.5	µs	During drain charge

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	$H\phi_1$, $H\phi_2$	8	10		ns	

Spectral Sensitivity Characteristics (excludes lens characteristics and light source characteristics)

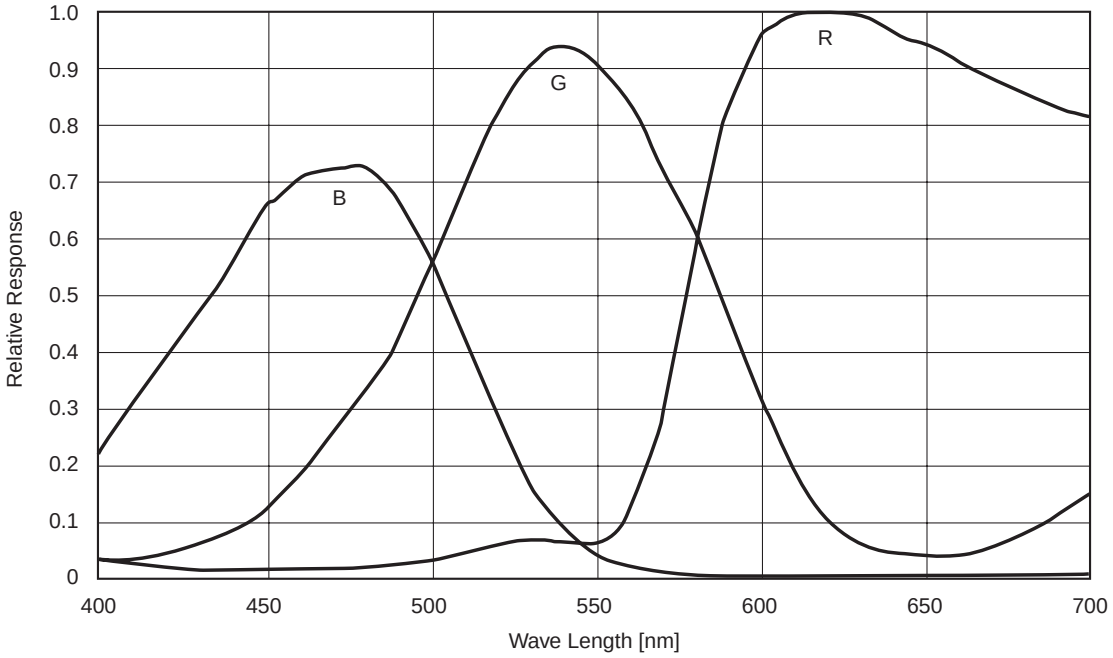
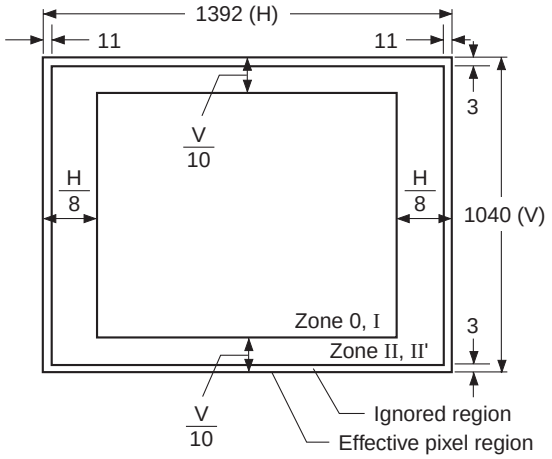


Image Sensor Characteristics (Ta = 25°C)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G Sensitivity		Sg		1240		mV	1	1/30s accumulation
Sensitivity comparison	R	Rr	0.40	0.60	0.70		1	
	B	Rb	0.30	0.53	0.60			
Saturation signal		Vsat	850			mV	2	Ta = 60°C
Smear		Sm		–110	–100	dB	3	Progressive scan mode
				–98	–88			High frame rate readout mode
Video signal shading		SHg			20	%	4	Zone 0 and I
					25			Zone 0 to II'
Dark signal		Vdt			10	mV	5	Ta = 60°C, 15 frames/s
Dark signal shading		ΔVdt			4	mV	6	Ta = 60°C, 15 frames/s, *1
Line crawl G		Lcr			3.8	%	7	
Line crawl R		Lcg			3.8	%	7	
Line crawl B		Lcb			3.8	%	7	
Lag		Lag			0.5	%	8	

*1 Excludes vertical dark signal shading caused by vertical register high-speed transfer.

Zone Definition of Video Signal Shading



Measurement System

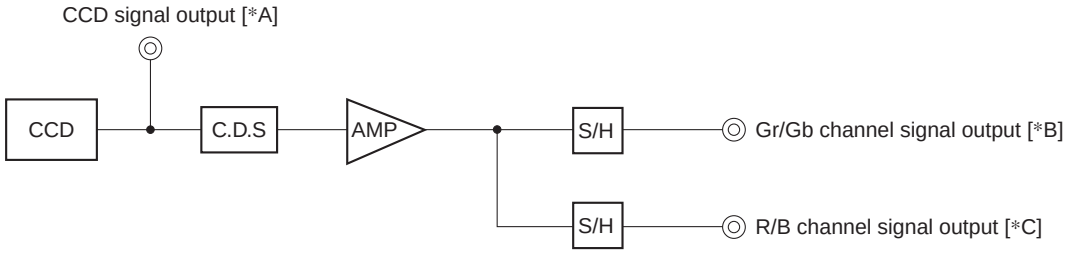
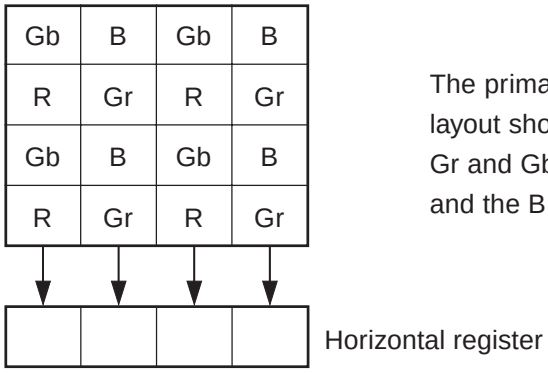


Image Sensor Characteristics Measurement Method

◎ Color coding of this image sensor & Readout



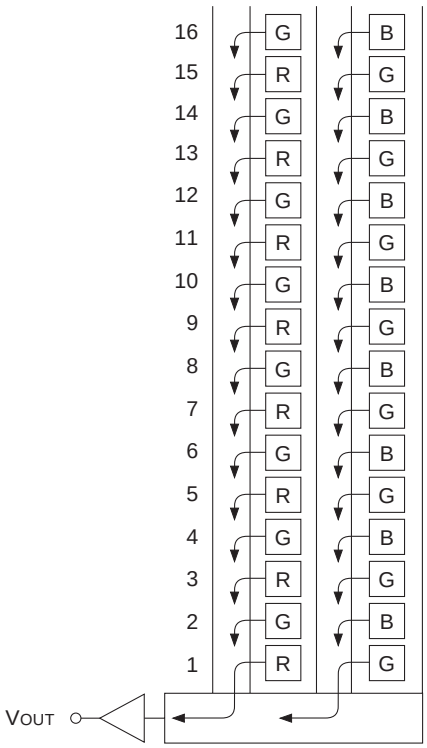
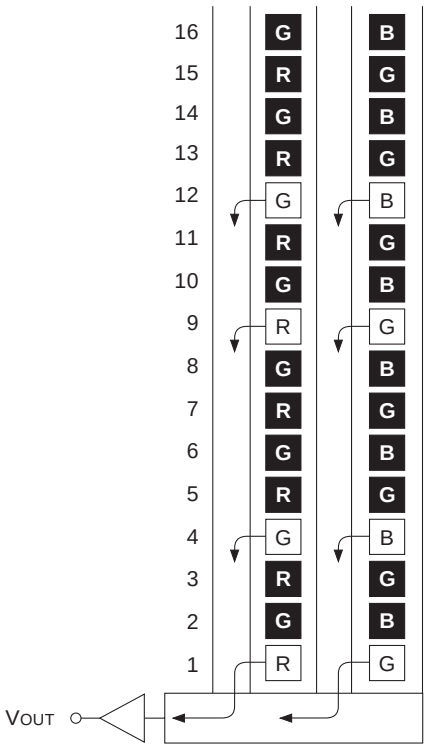
Color Coding Diagram

The primary color filters of this image sensor are arranged in the layout shown in the figure on the left (Bayer arrangement).
Gr and Gb denote the G signals on the same line as the R signal and the B signal, respectively.

All pixels' signals are output successively in a 1/15s period.
The R signal and Gr signal lines and the Gb signal and B signal lines are output successively.

◎ **Readout modes**

The output methods for the following two readout modes are shown below.

Progressive scan mode	High frame rate readout mode
	

Note) Blacked out portions in the diagram indicate pixels which are not read out.
Output starts from line 1 in high frame readout modes.

1. Progressive scan mode
   In this mode, all pixels' signals are output in non-interlace format in 1/15s.
   All pixels' signals within the same exposure period are read out simultaneously, making this mode suitable for high resolution image capturing.

2. High frame rate readout mode
   All effective areas are scanned in approximately 1/60s by reading out two out of eight lines (1st and 4th lines, 9th and 12th lines, and so on). The vertical resolution is approximately 256 TV-lines. This readout mode emphasizes processing speed over vertical resolution.

Image Sensor Characteristics Measurement Method

◎ **Measurement conditions**

(1) In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions, and the progressive scan mode is used.

(2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value of the Gr/Gb signal output or the R/B signal output of the measurement system.

◎ **Definition of standard imaging conditions**

(1) Standard imaging condition I:
Use a pattern box (luminance: 706cd/m^2, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

(2) Standard imaging condition II:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. Sensitivity, sensitivity comparison
Set to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100s, measure the signal outputs (V_{GR}, V_{Gb}, V_R and V_B) at the center of each Gr, Gb, R and B channel screen, and substitute the values into the following formulas.

$V_G = (V_{Gr} + V_{Gb}) /2$

$Sg = V_G \times \frac{100}{30}$ [mV]

$Rr = V_R/V_G$

$Rb = V_B/V_G$

2. Saturation signal
Set to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr signal output, 200mV, measure the minimum values of the Gr, Gb, R and B signal outputs.

3. Smear
Set to the standard imaging condition II. With the lens diaphragm at F5.6 to F8, first adjust the average value of the Gr signal output to 200mV. Measure the average values of the Gr signal output, Gb signal output, R signal output and B signal output (Gra, Gba, Ra, Ba), and then adjust the luminous intensity to 500 times the intensity with the average value of the Gr signal output, 200mV.
After the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (Vsm [mV]) independent of the Gr, Gb, R and B signal outputs, and substitute the values into the following formula.

$$Sm = 20 \times \log \left(Vsm \div \frac{Gra + Gba + Ra + Ba}{4} \times \frac{1}{500} \times \frac{1}{10} \right) \text{[dB]}$$ (1/10V method conversion value)

4. Video signal shading
   Set to the standard imaging condition III. With the lens diaphragm at F5.6 to F8, adjusting the luminous intensity so that the average value of the Gr signal output is 200mV. Then measure the maximum value (Grmax [mV]) and minimum value (Grmin [mV]) of the Gr signal output and substitute the values into the following formula.

   $SHg = (Grmax - Grmin) / 200 \times 100$ [%]

5. Dark signal
   Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature of 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

6. Dark signal shading
   After measuring 5, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

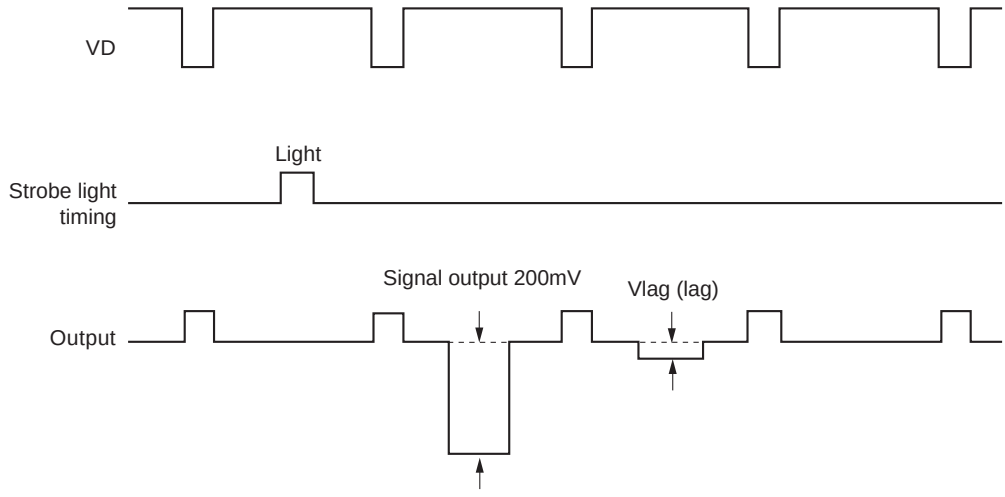
   $\Delta Vdt = Vdmax - Vdmin$ [mV]

7. Line crawl
   Set to the standard imaging condition II. Adjusting the luminous intensity so that the average value of the Gr signal output is 200mV, and then insert R, G and B filters and measure the difference between G signal lines (ΔGlr, ΔGlg, ΔGlb [mV]) as well as the average value of the G signal output (Gar, Gag, Gab). Substitute the values into the following formula.

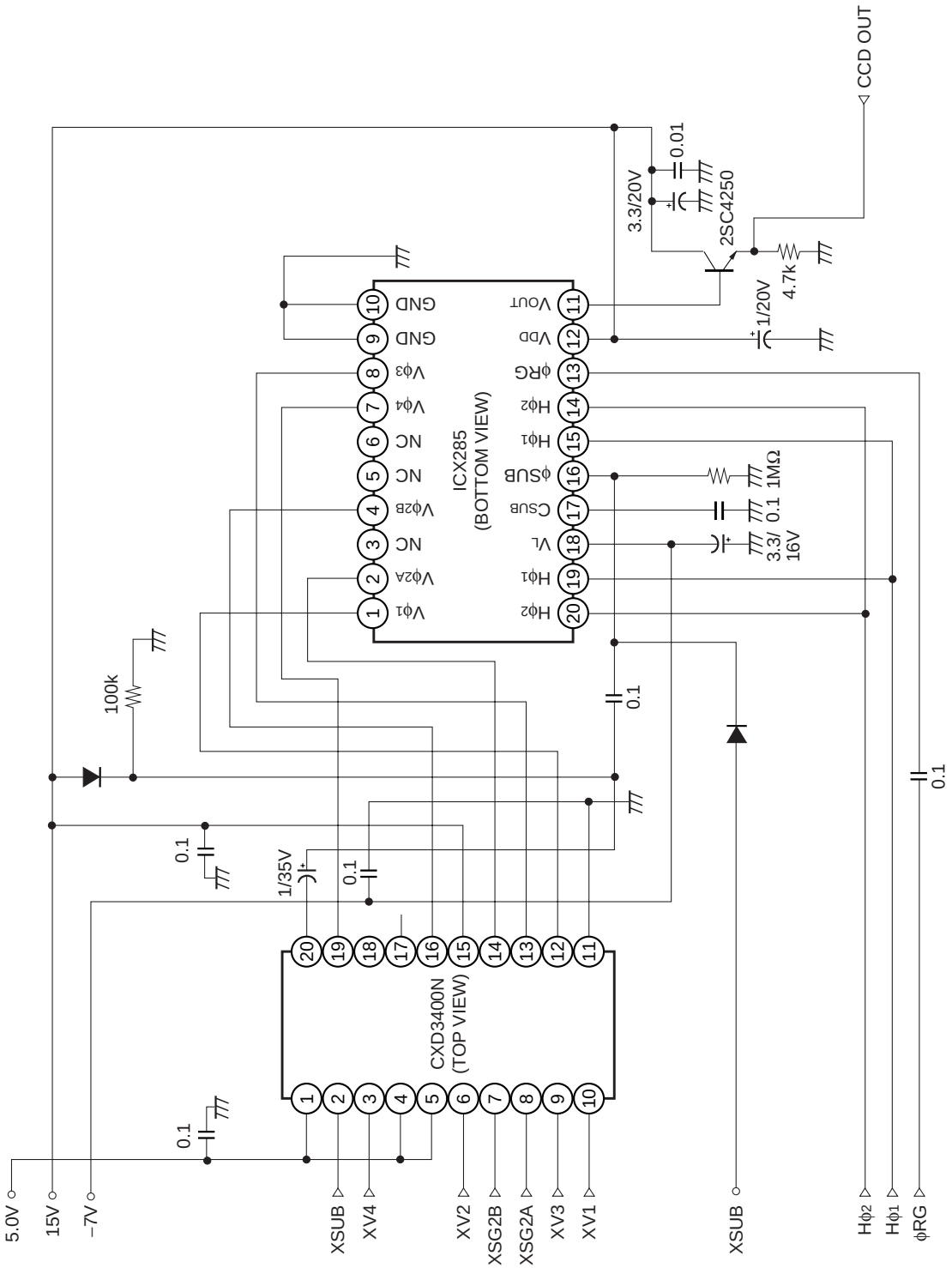
   $$Lci = \frac{\Delta Gli}{Gai} \times 100 \text{ [\%]} \quad (i = r, g, b)$$

8. Lag
   Adjust the Gr signal output value generated by the strobe light to 200mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal amount (Vlag). Substitute the value into the following formula.

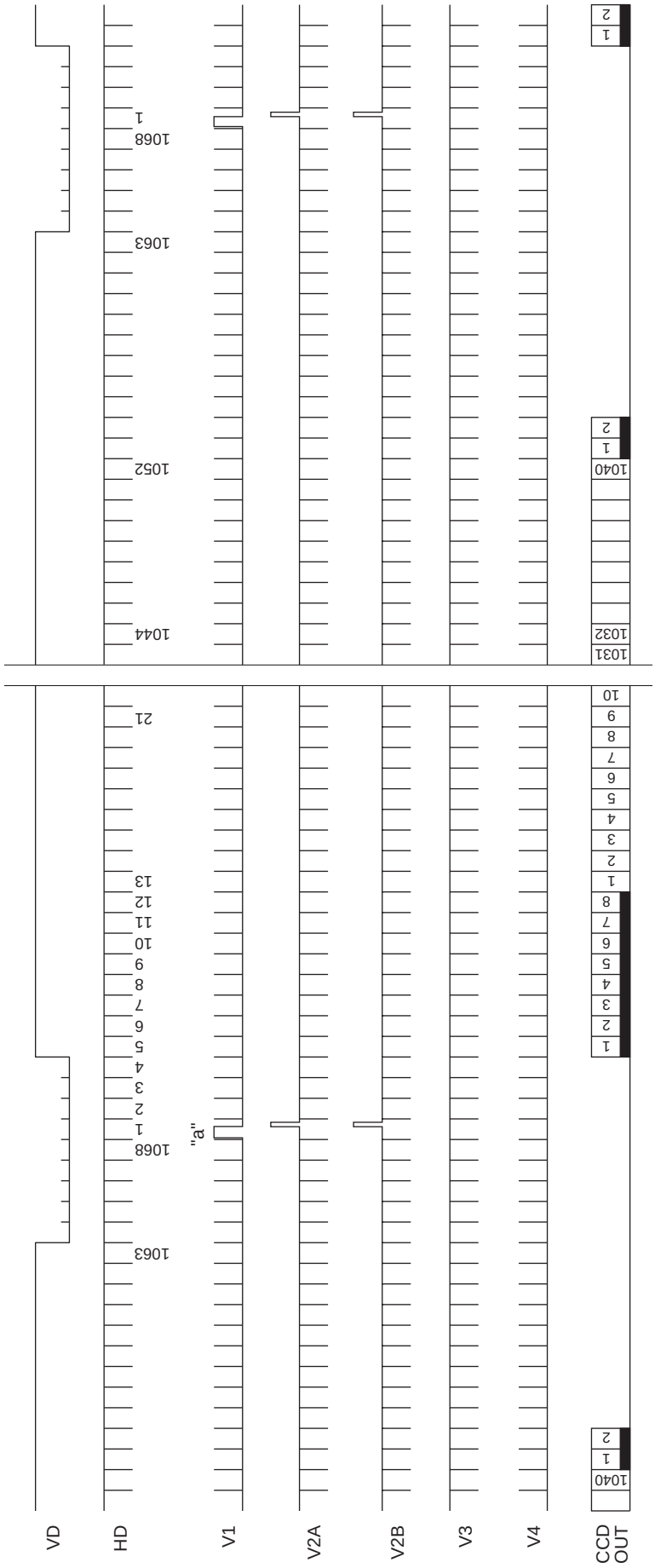
   $Lag = (Vlag/20) \times 100$ [%]



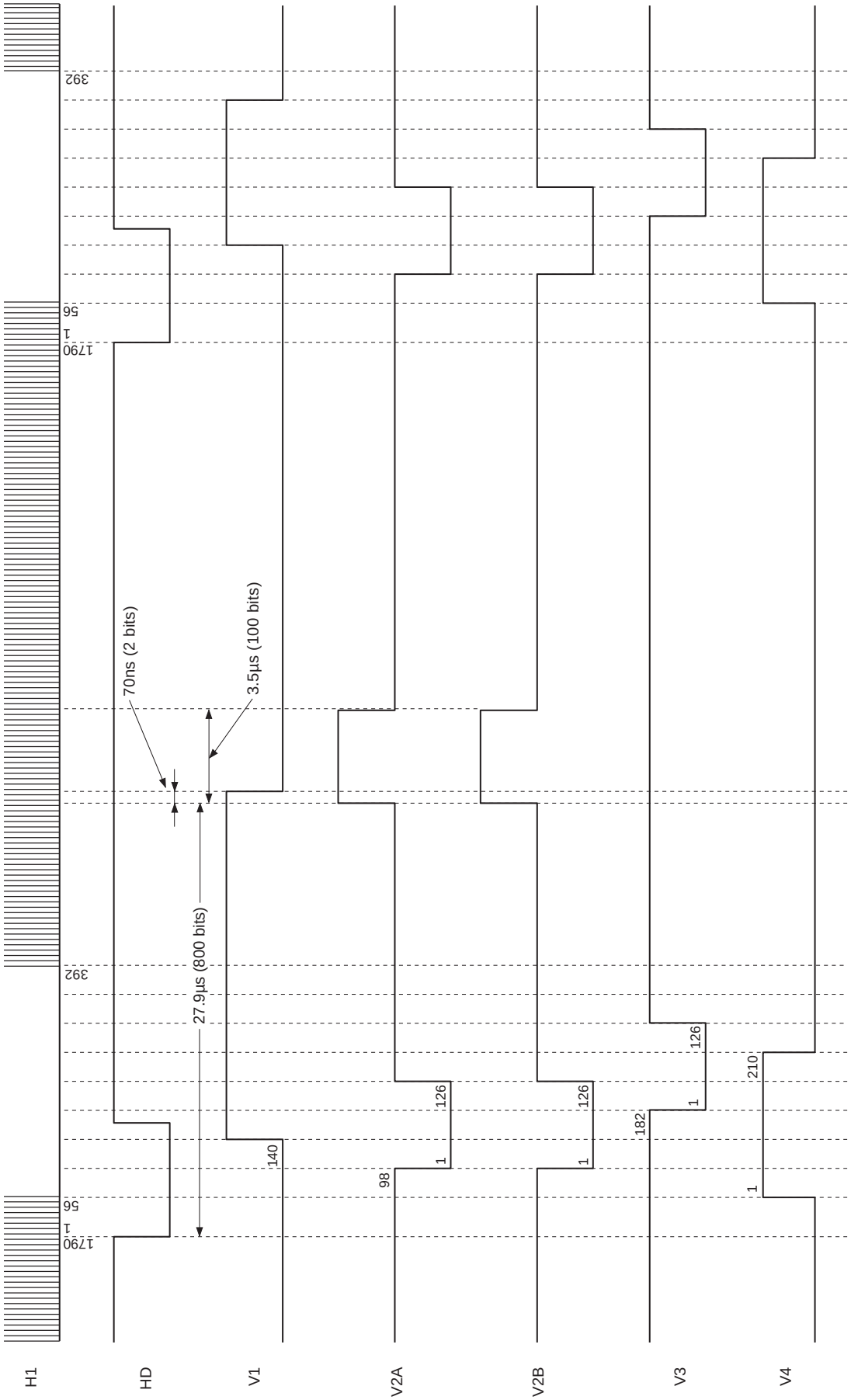
Drive Circuit



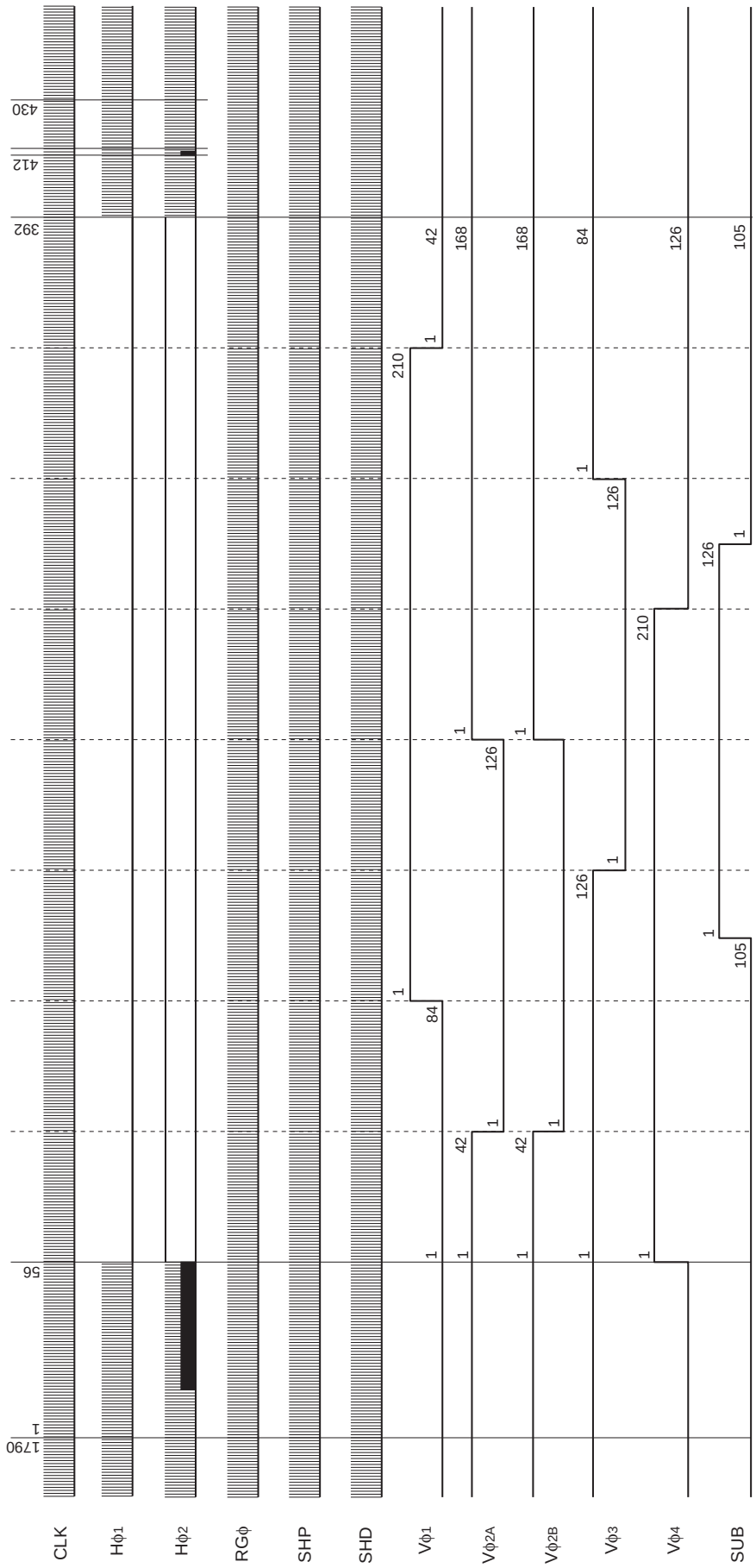
Drive Timing Chart (Vertical Sync) Progressive Scan Mode



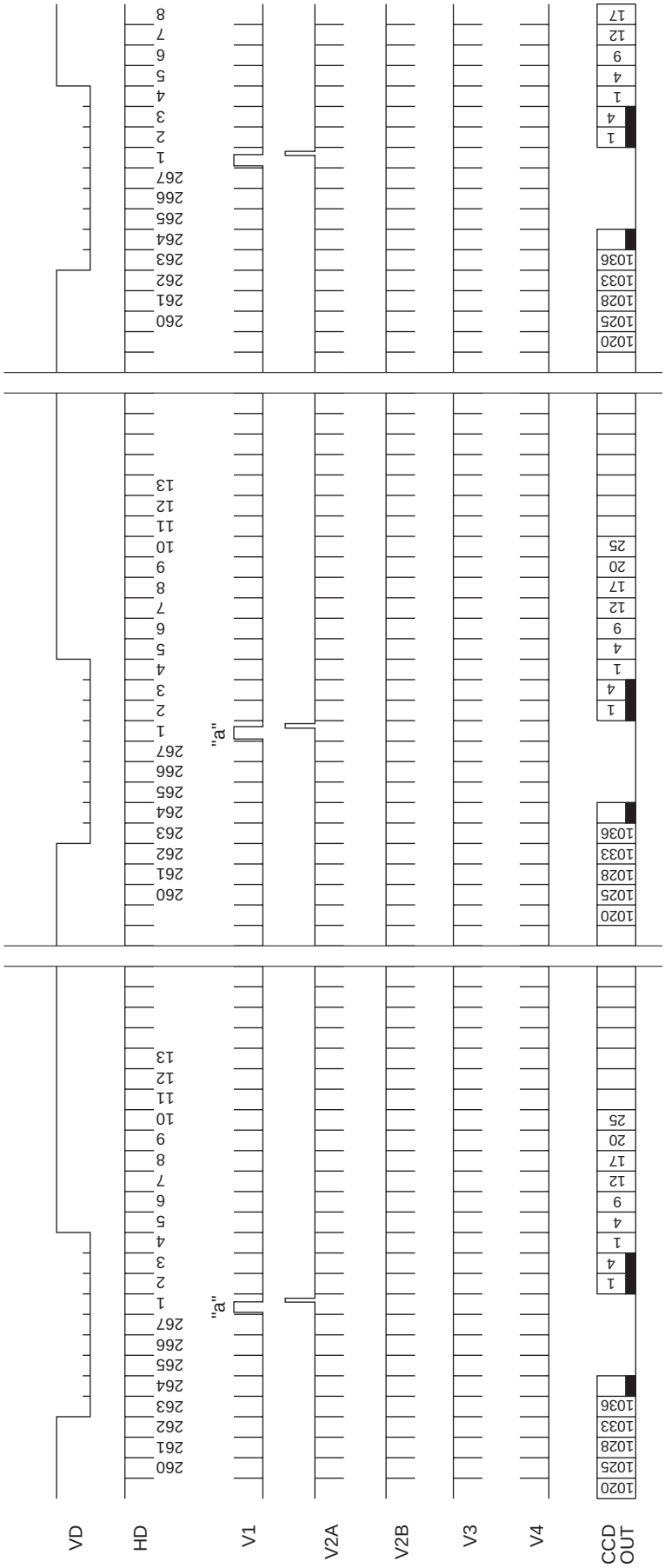
Drive Timing Chart (Vertical Sync "a" Enlarged) Progressive Scan Mode



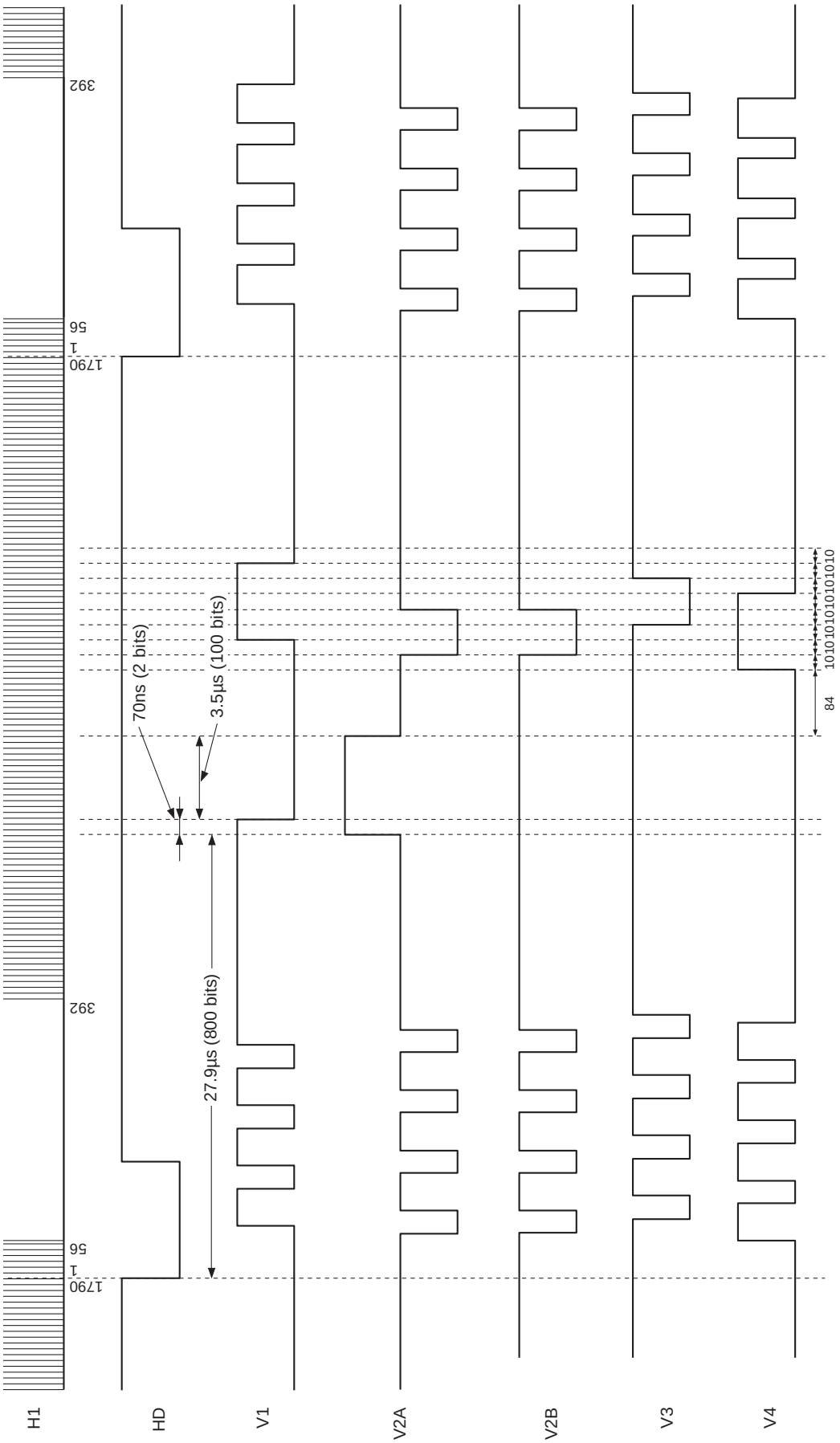
Drive Timing Chart (Horizontal Sync) Progressive Scan Mode



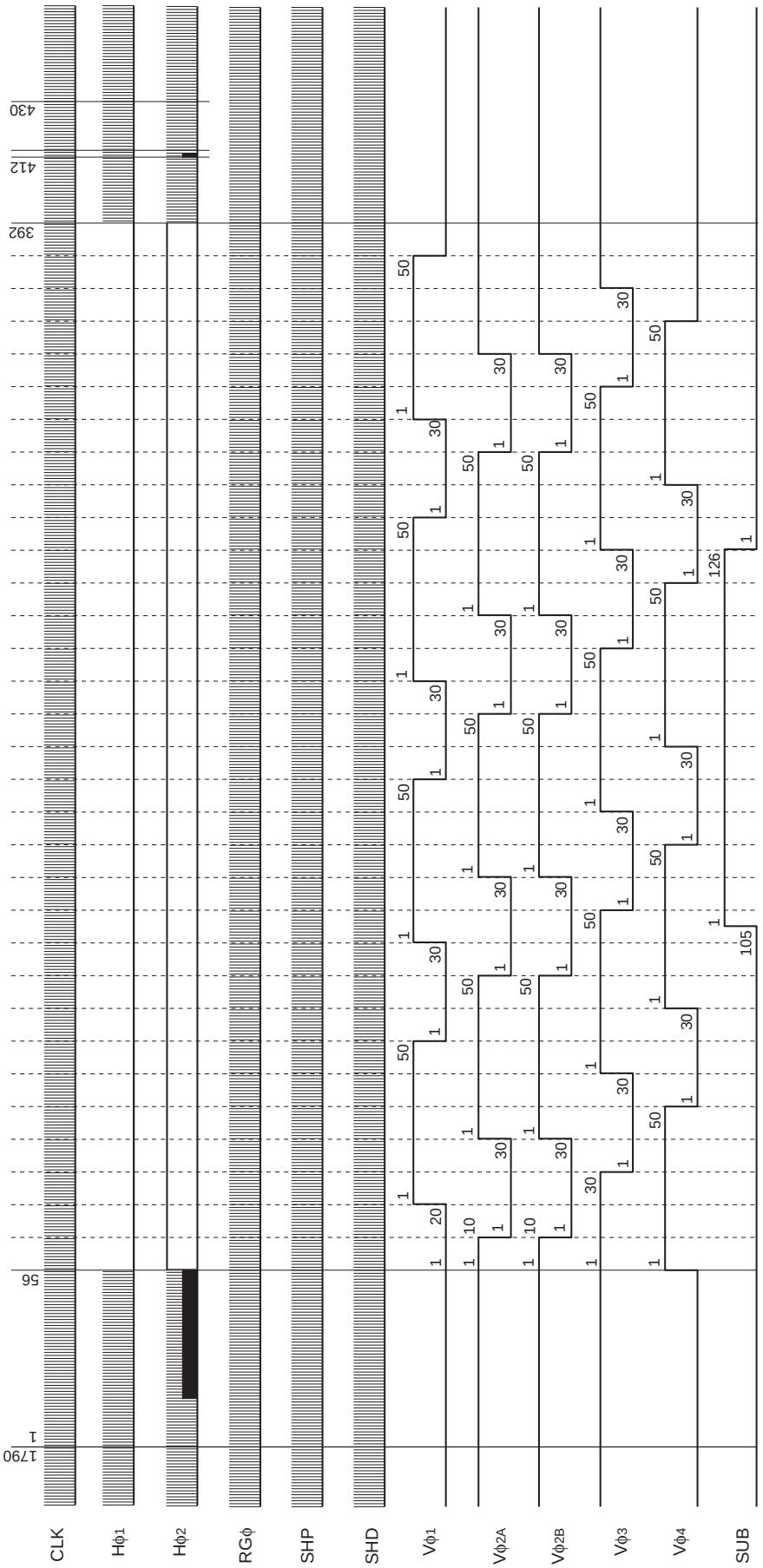
Drive Timing Chart (Vertical Sync) High Frame Rate Readout Mode



Drive Timing Chart (Vertical Sync "a" Enlarged) High Frame Rate Readout Mode



Drive Timing Chart (Horizontal Sync) High Frame Rate Readout Mode



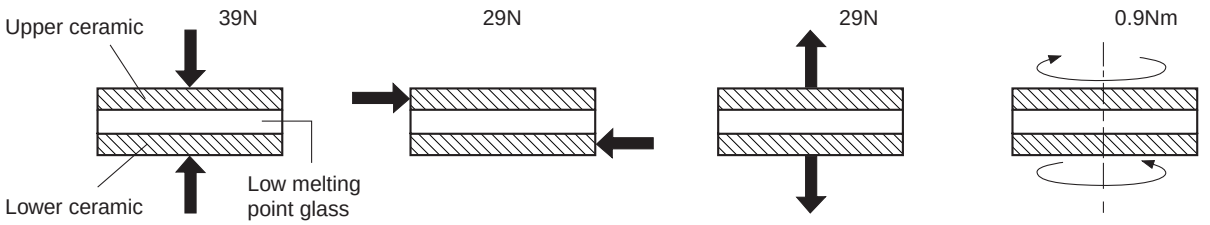
Notes on Handling

1) Static charge prevention
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non-chargeable gloves, clothes or material. Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensors.
   e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering toll, use a thermal controller of the zero-cross On/Off type and connect it to ground.

3) Dust and dirt protection
Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operations as required, and use them.
   a) Perform all assembly operations in a clean room (class 1000 or less).
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Installing (attaching)
   a) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply and load or impact to limited portions. (This may cause cracks in the package.)



   b) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use an elastic load, such as a spring plate, or an adhesive.

c) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to other locations as a precaution.

d) The upper and lower ceramic are joined by low melting point glass. Therefore, care should be taken not to perform the following actions as this may cause cracks.
   - Applying repeated bending stress to the outer leads.
   - Heating the outer leads for an extended period with a soldering iron.
   - Rapidly cooling or heating the package.
   - Applying any load or impact to a limited portion of the low melting point glass using tweezers or other sharp tools.
   - Prying at the upper or lower ceramic using the low melting point glass as a fulcrum. Note that the same cautions also apply when removing soldered products from boards.

e) Acrylate anaerobic adhesives are generally used to attach CCD image sensors. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives. (reference)

5) Others

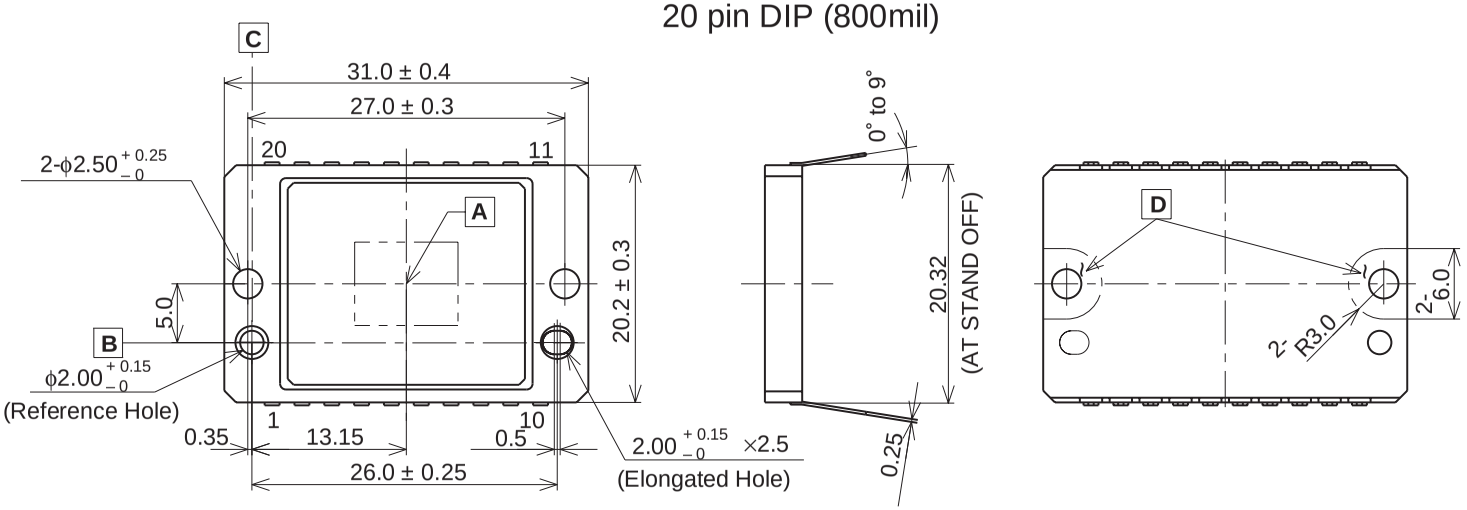
a) Do not expose to strong light (sun rays) for long periods, as color filters will be discolored. When high luminous objects are imaged with the exposure level controlled by the electronic iris, the luminance of the image-plane may become excessive and discoloring of the color filter will possibly be accelerated. In such a case, it is advisable that taking-lens with the automatic-iris and closing of the shutter during the power-off mode should be properly arranged. For continuous using under cruel condition exceeding the normal using condition, consult our company.

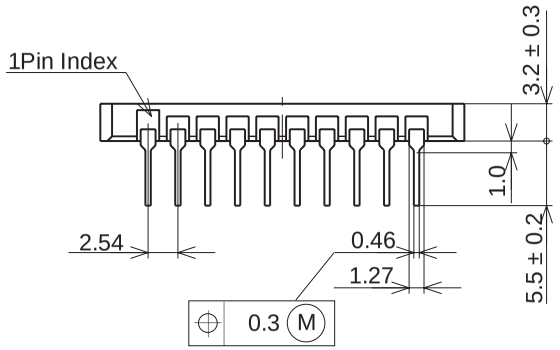
b) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

c) This CCD image sensor has a device structure that is sensitive to near infrared light, so white spots during the subsequent dark signal occur at a higher probability compared to CCD image sensors with normal structures. Therefore, note that the white spot at dark signal specification cannot be guaranteed when used after storage for long periods.

Package Outline Unit: mm

20 pin DIP (800mil)





1. "**A**" is the center of the effective image area.
2. The straight line **"B"** which passes through the center of the reference hole and the elongated hole is the reference axis of vertical direction (V).
3. The straight line **"C"** which passes through the center of the reference hole at right angle to vertical reference line **"B"** is the reference axis of horizontal direction (H).
4. The bottom **"D"** is the height reference.(Two points are specified.)
5. The center of the effective image area specified relative to the reference hole is (H, V) = (13.15, 5.0) ± 0.15mm.
6. The angle of rotation relative to the reference line **"B"** is less than ± 1°
7. The height from the bottom **"D"** to the effective image area is 1.46 ± 0.15mm.
8. The tilt of the effective image area relative to the bottom **"D"** is less than 60µm.
9. The thickness of the cover glass is 0.75mm and the refractive index is 1.5.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	5.90g
DRAWING NUMBER	AS-A11(E)